What is claimed is:

1. A nonvolatile semiconductor memory device comprising:

a semiconductor substrate comprising an active region and an isolation region;

1-byte memory transistors arranged in a first direction, wherein each of the 1-byte memory transistors includes a junction region and a channel region formed in the active region of the semiconductor substrate; and

a byte select transistor disposed in the active region, wherein the byte select transistor includes a junction region that is directly adjacent to the junction of each of the 1-byte memory transistors.

2. The device of claim 1, wherein the byte select transistor is disposed over or under the 1-byte memory transistors perpendicular to the arranged direction of the 1-byte memory transistors.

3. The device of claim 1, wherein the junction of each of the 1-byte memory transistors that is directly adjacent to the junction of the byte select transistor is a source region.

4. The device of claim 1, wherein the junction of the byte select transistor that is directly adjacent to the junction of each of the 1-byte memory transistors is a drain region.

5. The device of claim 1, wherein the junction region and a channel region of the byte select transistor are disposed in an undoped native semiconductor substrate.

6. The device of claim 1, wherein the junction region and a channel region of the byte select transistor are disposed in a doped conductive well region.

7. The device of claim 6, wherein the junction region and a channel region of each of the 1-byte memory transistors are disposed in the doped conductive well region.

8. The device of claim 1, wherein each of the 1-byte memory transistors is a device operating according to source side injection.

9. The device of claim 1, wherein the width of a channel region of the byte select transistor is larger than the sum of the widths of channel regions of the 1-byte memory transistors.

10. The device of claim 9, wherein the width of the channel region of the byte select transistor is equal to or larger than the sum of the widths of the channel regions of the 1-byte memory transistors and the widths of the isolation regions between adjacent 1-byte memory transistors.

11. The device of claim 1, wherein each of the 1-byte memory transistors is a floating-gate-type transistor.

12. The device of claim 1, wherein each of the 1-byte memory transistors is a silicon-oxide-nitride-oxide-silicon-type transistor or a metal-oxide-nitride-oxide-silicon-type transistor.

13. The device of claim 12, wherein a gate electrode structure of the silicon-oxide-nitride-oxide-silicon-type transistor or the metal-oxide-nitride-oxide-silicon-type transistor includes a first oxide layer, a nitride layer, a second oxide layer, and a conductive layer, which are sequentially stacked and have substantially the same width.

14. The device of claim 12, wherein:

a gate electrode structure of the silicon-oxide-nitride-oxide-silicon-type transistor or the metal-oxide-nitride-oxide-silicon-type transistor includes a first oxide layer, a nitride layer, a second oxide layer, and a conductive layer stacked sequentially;

the first oxide layer, the second oxide layer, and the conductive layer have substantially the same width; and

the nitride layer has a width smaller than the first oxide layer, the second oxide layer, and the conductive layer.

15. A byte-operational nonvolatile semiconductor memory device including a plurality of byte memory cells, each of which comprises:

a memory cell block including 1-byte memory transistors arranged in one direction; and

a byte-operational block including a byte select transistor and disposed over or under the memory cell block and perpendicular to the direction in which the 1-byte memory transistors are arranged.

16. The device of claim 15, further comprising:

a plurality of bit lines, which are electrically connected to drain regions of the 1-byte memory transistors, respectively;

a plurality of global source lines, which are electrically connected to a source region of the byte select transistor;

a plurality of word lines, which are connected to gate lines of the 1-byte memory transistors, respectively; and

a plurality of byte select lines, which are connected to a gate electrode of the byte select transistor,

wherein a source region of each of the 1-byte memory transistors and a drain region of the byte select transistor constitute a shared junction region.

17. The device of claim 16, wherein the word lines and the byte select lines are disposed parallel to each other.

18. The device of claim 16, wherein the shared junction region is disposed in a doped conductive well region.

19. The device of claim 16, wherein a part of the shared junction region is disposed in a doped conductive well region and the other part of the shared junction region is disposed in a native semiconductor substrate.

20. The device of claim 15, wherein the source region, the drain region, and a channel region of the byte select transistor are disposed in an undoped native semiconductor substrate.

21. The device of claim 15, wherein the source region, the drain region, and a channel region of the byte select transistor are disposed in a doped conductive well region.

22. The device of claim 21, wherein the source region, the drain region, and a channel region of each of the 1-byte memory transistors are disposed in the doped conductive well region.

23. The device of claim 15, wherein each of the 1-byte memory transistors is a device operating through source side injection.

24. The device of claim 15, wherein the width of a channel region of the byte select transistor is larger than the sum of the widths of channel regions of the 1-byte memory transistors.

25. The device of claim 15, wherein each of the 1-byte memory transistors is a floating-gate-type transistor.

26. The device of claim 15, wherein each of the 1-byte memory transistors is a silicon-oxide-nitride-oxide-silicon-type transistor or a metal-oxide-nitride-oxide-silicon-type memory transistor.

27. The device of claim 26, wherein a gate electrode structure of the silicon-oxide-nitride-oxide-silicon-type transistor or the metal-oxide-nitride-oxide-silicon-type memory transistor includes a first oxide layer, a nitride layer, a second oxide layer, and a conductive layer, which are sequentially stacked and have the same width.

28. The device of claim 26, wherein:

a gate electrode structure of the silicon-oxide-nitride-oxide-silicon-type transistor or the metal-oxide-nitride-oxide-silicon-type memory transistor includes a first oxide layer, a nitride layer, a second oxide layer, and a conductive layer, which are sequentially stacked;

the first oxide layer, the second oxide layer, and the conductive layer have substantially the same width; and

the nitride layer has a width less than the width of the first oxide layer, the second oxide layer, and the conductive layer.

29. An apparatus comprising a memory cell, wherein the memory cell comprises:

a plurality of first transistors configured to store data; and

a second transistor configured to activate the plurality of first transistors at the same time, wherein:

a source or a drain of each of the plurality of first transistors is connected to a source or a drain of the second transistor;

the resistance of each connection between each of the plurality of first transistors and the second transistor is substantially the same.

30. The apparatus of claim 29, wherein the length of each connection between each of the plurality of first transistors and the second transistor is substantially the same.

31. The apparatus of claim 30, wherein the length of each connection between each of the plurality of first transistors and the second transistor is minimized.

32. The apparatus of claim 29, wherein:

the plurality of first transistors are arranged parallel to each other in a row;

a channel of the second transistor is substantially parallel to each channel of each of the plurality of first transistors.

33. The apparatus of claim 32, wherein the channel width of the second transistor extends approximately the length of the row of the plurality of first transistors.

34. The apparatus of claim 33, wherein each connection between each of the plurality of first transistors and the second transistor is at a different point along

the source or the drain of the second transistor.

35. The apparatus of claim 29, wherein the apparatus is comprised in a NOR-type flash memory device utilizing source side injection during operation.

36. The apparatus of claim 29, wherein the plurality of first transistors comprise at least three transistors.

37. The apparatus of claim 36, wherein the plurality of first transistors comprise eight transistors.